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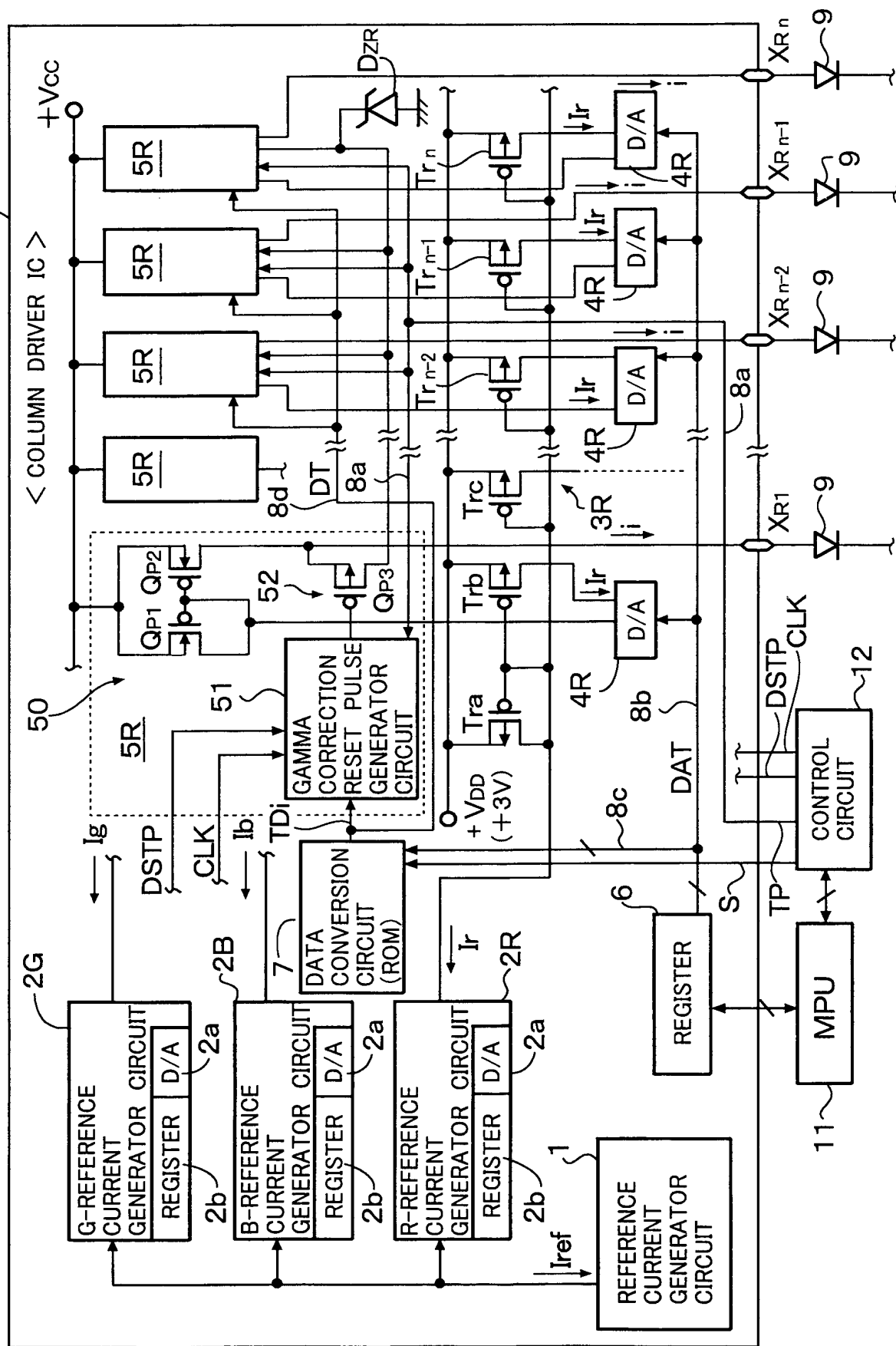


FIG. 2

The diagram shows the internal structure of the control circuit 12, which includes a timing signal generator circuit 12a. The timing signal generator circuit 12a outputs four signals: CLK, DSTP, CSTP, and Tp. The control circuit 12 is connected to the data conversion circuit 7 via a signal line S. The data conversion circuit 7 outputs a signal TDi to the preset counter. The preset counter is connected to the D input of a flip-flop (F/F). The flip-flop also has a reset input (R) connected to a resistor network between +VDD and ground, and a clock input (Q) connected to the output of an inverter (55). The inverter 55 is connected to the output of the flip-flop (Q) and the output of the preset counter. The output of the inverter 55 is connected to the gate of a PMOS transistor (QP3) and the anode of a diode (DZR). The cathode of the diode (DZR) is connected to ground. The output of the PMOS transistor (QP3) is connected to the output of the data conversion circuit 7 via a signal line 54. The output of the data conversion circuit 7 is also connected to the output of the PMOS transistor (QP3) via a signal line 51. The output of the PMOS transistor (QP3) is connected to the output of the data conversion circuit 7 via a signal line 52.

[illegible]

FIG. 4(a)

- TIMING CONTROL PULSE T_P
- FIRST STAGE OUTPUT OF SHIFT REGISTER 56
- SECOND STAGE OUTPUT OF SHIFT REGISTER 56
- THIRD STAGE OUTPUT OF SHIFT REGISTER 56
- FOURTH STAGE OUTPUT OF SHIFT REGISTER 56

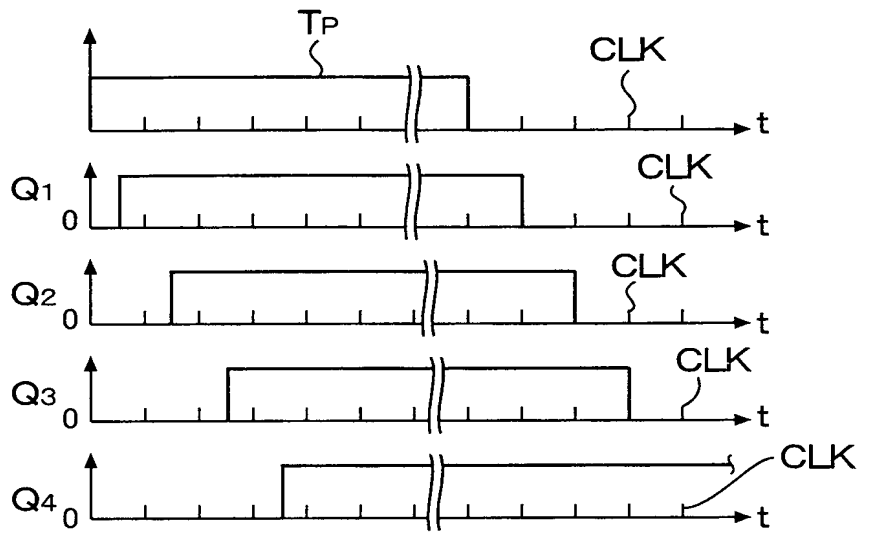


FIG. 4(b)

- TIMING CONTROL PULSE T_P
- THIRD STAGE OUTPUT OF SHIFT REGISTER 56
- OUTPUT OF AND GATE 58

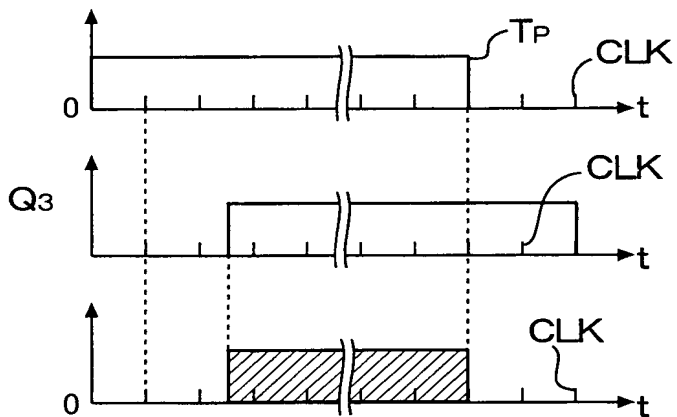


FIG. 5

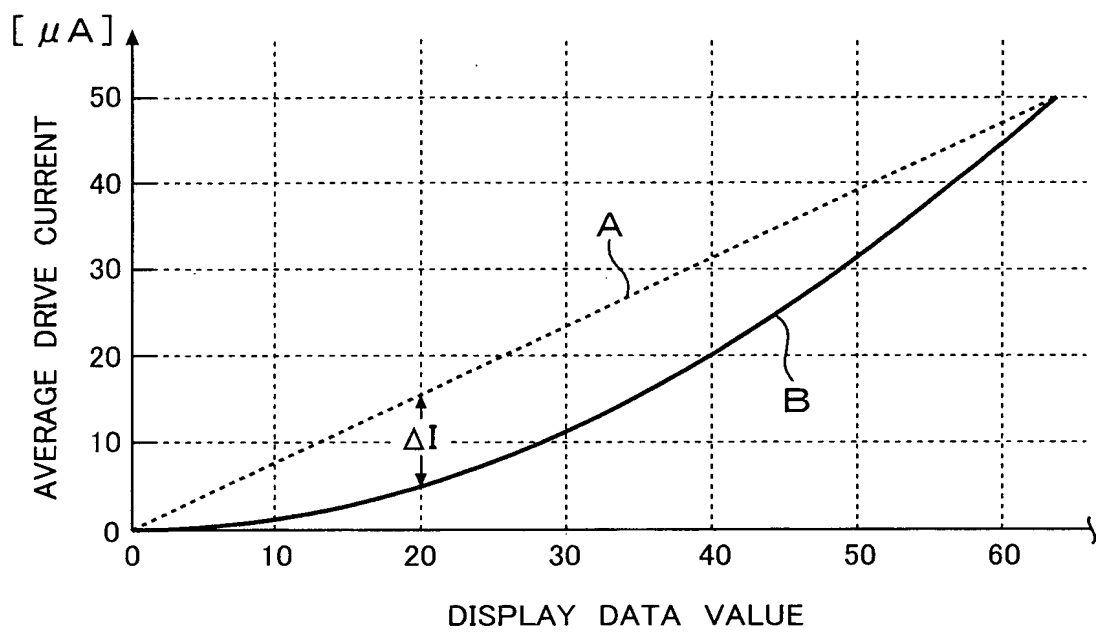


FIG. 6

